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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/577,486	04/27/2006	Tomoyuki Kanno	136163	5122
25944 7590 12/19/2008 OLIFF & BERRIDGE, PLC P.O. BOX 320850 ALEXANDRIA, VA 22320-4850				
EXAMINER				
BEHM, HARRY RAYMOND				
ART UNIT		PAPER NUMBER		
2838				
MAIL DATE		DELIVERY MODE		
12/19/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action
Before the Filing of an Appeal Brief

Application No.

10/577,486

Applicant(s)

KANNO, TOMOYUKI

Examiner

HARRY BEHM

Art Unit

2838

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 02 December 2008 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.
b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
(a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
(b) ☐ They raise the issue of new matter (see NOTE below);
(c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
The status of the claim(s) is (or will be) as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____.
Claim(s) rejected: 1 and 3.
Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
see the continuation of 11 below.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Akm Enayat Ullah/
Supervisory Patent Examiner, Art Unit 2838

Continuation of 11 above:

Response to Arguments

Applicant's arguments filed 12/2/08 have been fully considered but they are not persuasive.

Applicant argues Ohsawa in view of Bonnet fails to disclose connecting both the inverter circuit and the voltage doubler circuit to the booster. However, Kassapian teaches it was well known to connect an inverter circuit input Phi1 and a voltage doubler circuit input Vcc to a booster. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant further argues Kassapian fails to disclose a booster circuit capable of receiving two different input signals. However, Kassapian clearly discloses a booster circuit receiving a first input Vcc and a second input Phi1. Applicant further argues input Phi1 is merely a clock input signal. However, the output of a half-bridge inverter circuit is also a square wave identical to signal Phi1 as shown in Figure 3.

Applicant argues the combination fails to operate in the manner intended by the present disclosure. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., manner intended in the present disclosure) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Finally, Applicant argues adding a voltage doubler would fail to achieve a desired result because of the choice of the secondary side ground terminal of Ohsawa. However, the choice of the connection point of a ground reference does not alter the AC voltage seen by the load.

Since the voltage drop across the load is the same whether the doubler doubles 'up' to positive twice the input voltage or double 'down' to negative twice the input voltage, the selection of the ground point is largely arbitrary. Applicant argues if the voltage doubler were across Ohsawa's diode 5, the doubler would shift the input voltage by 0, while if the voltage doubler were across diode 6, the voltage shift would be negative. However, one of ordinary skill in the art could implement either a positive voltage doubler across diode 5 or a negative voltage doubler across diode 6, depending on the choice of ground, and the voltage drop across the load would be unchanged. Contrary to Applicant's assertion, implementing a negative voltage doubler to reduce rather than raise the voltage would not be undesirable and would not alter the voltage drop across the load. Ohsawa discloses negative voltage doubling, Kassapian discloses positive voltage doubling and Bonnet does not disclose the ground connection point. Both negative and positive voltage doubling were well known in the art and Applicant's claim language does not preclude either doubling method.